REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-13. Specifically, the Office Action rejected claims 1-13 under 35 U.S.C. 102(b), as being anticipated by Chen et al. (U.S. 6,351,364). Applicants have amended claims 1 and 7 to improve clarity. After entry of the foregoing amendments, claims 1-13 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The Applicant's invention is directed to an electrostatic discharge (ESD) device used with a high-voltage input pad is described. The ESD device serves as a secondary device of a two-stage protection circuit, and comprises a substrate, a first MOS transistor and a second MOS transistor. The first MOS transistor is disposed on the substrate and comprises a first gate, a first drain and a first source, wherein the first gate is coupled to a bias Vg1, and the first drain is coupled to the high-voltage input pad. The second MOS transistor is disposed on the substrate and comprises a second gate, a second drain and a second source, wherein the second gate and the second source are both grounded, and the second drain is electrically connected with the first source of the first MOS transistor.

Discussion of Office Action Rejections

The Office Action rejected claims 1-13 under 35 U.S.C. 102(b), as being anticipated by Chen et al. (U.S. 6,351,364). Applicants respectfully traverse the rejections for at least the reasons set forth below.

The features of the invention are recited in claims 1, and 7. Independent claims 1, 7 recited the features and recites the features as follows:

1. An electrostatic discharge (ESD) device used with a high-voltage input pad, wherein the ESD device is disposed between the high-voltage input pad and an internal circuit, comprising:

a primary device disposed on a substrate, wherein the primary device is coupled to the high-voltage input pad and the internal circuit; and

a secondary device disposed on the substrate between the primary device and the internal circuit, wherein the second device comprising:

a first MOS transistor comprising a first gate, a first drain and a first source, wherein the first gate is coupled to a bias Vg1, and the first drain is coupled to the high-voltage input pad; and

a second MOS transistor comprising a second gate, a second drain and a second source, wherein the second gate and the second source are both grounded, and the second drain is electrically connected with the first source of the first MOS transistor.

10. A programmable memory apparatus, comprising:

a substrate;

a programmable memory device on the substrate;

a high-voltage input pad on the substrate electrically connected with the memory device; and

a two-stage protection circuit disposed on the substrate and coupled between the memory device and the high-voltage input pad, ***the two-stage protection circuit comprising a primary device and a secondary device, wherein the secondary device is disposed between the primary device and the programmable memory device, and*** the secondary device comprises:

a first MOS transistor disposed on the substrate, comprising a first gate, a first drain and a first source, wherein the first gate is coupled to a bias Vg1, and the first drain is coupled to the high-voltage input pad; and

a second MOS transistor disposed on the substrate, comprising a second gate, a second drain and a second source, wherein the second gate and the second source are both grounded, and the second drain is electrically connected with the first source of the first MOS transistor.

Chen discloses an ESD protective circuit 30 comprising three NMOS transistors 36, 38 and 40 and two PMOS transistors 42, 44 (Fig 2). The NMOS transistor 36 has a drain terminal coupled to the I/O pad 32, a gate terminal coupled to a voltage source VDD and a source terminal coupled to a drain terminal of the NMOS transistor 38. The NMOS transistor 38 has a gate and a source terminal coupled to the ground voltage VSS. The NMOS transistor 40 has a source terminal coupled to the I/O pad 32, a gate and a substrate terminal coupled to the ground voltage VSS and a drain terminal coupled to a substrate terminal of the PMOS transistor 44. PMOS transistor 42 has a source and a substrate terminal coupled to the I/O pad 32 and a gate terminal coupled to the voltage source VDD. The PMOS transistor 44 has a source and a gate terminal coupled to the voltage source VDD and a drain terminal coupled to the I/O pad 32. The resistor 46 is disposed between the voltage source VDD and the substrate of the PMOS transistor 44. The resistor 48 is disposed between the ground voltage source VSS and the substrate of the NMOS transistor 38.

The ESD device of the present invention comprises a primary device and a secondary device, wherein the secondary device is disposed between the primary device and the internal circuit. In detail, the secondary device disposed between the primary device and the internal

circuit of the present invention comprises a first NMOS transistor and a second NMOS transistor. However, in Chen's reference, the circuit near the internal circuit is composed of the PMOS transistor 42 and the NMOS transistor 40, and the circuit near the pad 32 is a cascade ESD protective circuit composed of the NMOS transistor 36, the NMOS transistor 38 and the PMOS transistor 44. Therefore, the ESD circuit of Chen is different from the present invention.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 7 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-6 and 8-13 patently define over the prior art as well.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-13 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw